

REMARKS

Reconsideration of the above-indicated patent application, as amended, is respectfully requested. The present amendment is responsive to the Non-Final Office Action mailed June 10, 2003. Claims 1-41 have been rejected. Accordingly, amended claims and supporting remarks are hereby presented that particularly point out and distinctly claim the subject matter that applicant regards as his invention. No new matter has been added.

THE INVENTION

The present invention includes embodiments directed to a system of data transfer between a first processing device and a second processing device, preferably a physical layer processor and a media access control layer processor as used with transferring data between wireless RF signals and electronic network signals. The present system speeds data transfer by eliminating intermediate storage steps. A plurality of memory storage devices are provided between the first and second processing devices for the purpose of synchronization and alignment. One of the memory storage devices is intermediate to the physical layer processor and the medium access control (MAC) layer processor.

In accordance with a first embodiment of the present invention, a new processor instruction running on the MAC processor is provided to implement a data transfer function for transferring data directly between a first memory storage device and a main memory storage device, without intermediate storage in a processor general purpose register or additional memory copy. This makes the MAC processor capable of accessing the PHY first memory storage device directly as an instruction operand, much like a conventional processor accesses it's general

purpose registers. This tight coupling of data transfer allows the MAC processor to efficiently parse and interrogate the header portion of the packet to extract the information it needs. MAC header processing is a very time critical operation which is optimized in the present invention, since data can be accessed natively by the MAC processor rather than dealing with the latency associated with additional intermediate memory transfers to access the header data. Thereafter when header processing is done, the MAC processor will direct the data payload portion (used by Host and not used by the MAC layer) to be transferred between the first memory storage device to a host memory storage device for further processing by a MAC processor. In accordance with a second embodiment of the present invention, data payload portion is efficiently transferred directly in a streaming fashion between a first memory storage device and the main memory storage device, without intermediate storage in either a processor register or a second memory storage device resident on the MAC processor. The present claims have been amended to explicitly recite these details such that the present claimed invention is very different from the prior art of record.

THE REJECTIONS UNDER 35 U.S.C. §102

Claims 1-41 had been rejected under Section 102(e) as allegedly being anticipated by Sandorfi (U.S. Pat. No. 5,768,530). This rejection is respectfully traversed, particularly as applied to the amended claims as presented herewith.

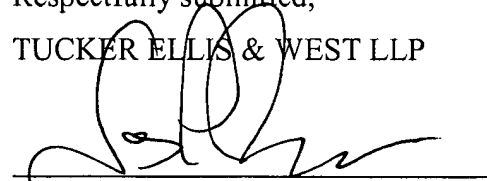
Sandorfi is directed to an application-specific integrated circuit (ASIC) used for providing an interface between different type buses with different characteristics, such as between a data processing system PCI bus and a fiber channel. (See col. 1, lines 30 et seq.) The ASIC of Sandorfi is thus clearly intended for processing frames between a high-speed data

channel and a diversity of interfaces. It is noted that Sandorfi does not disclose any specifics that would be applicable to an RF application, such as is the case with the present method and apparatus. In particular, the present claims now stipulate that data is received from a physical layer (PHY) processing system, which is understood to be in connection with radio frequency components. The present claims also stipulate that a single program instruction is executed on a media access control layer processor, which is further understood to be in connection with transferring between wireless- data packets and electronic network packets. And the claims also now recite that the single program instruction is used to directly transfer stored data from the PHY layer interface to a main memory for header processing. Therefore the MAC directs the payload data to flow directly from PHY to the Host. In this way, the present system moves data quickly through the MAC layer to the host without intermediate storage. The present system is thus instruction-driven unlike previous-type systems, and the present processor is thus involved in its own instruction set. Hence it allows the MAC processor to efficiently process the header immediately as it comes out of the PHY, just as easily as some processor's use general purpose registers in their instruction set. These details are not disclosed in Sandorfi and cannot be inferred from this reference. Thus, it is apparent that Sandorfi cannot be relied upon to show anticipation of the present claims in accordance with Section 102. Reconsideration and withdrawal are respectfully requested.

In view of the above, it is believed that independent claims 1, 6, 10, 15, 19, 24, 28, 32, 36, 40 and 41 recite limitations that distinguish over the prior art. The dependent claims are believed to be allowable for at least the same reasons as the independent claims. Reconsideration and withdrawal of this grounds of rejection is therefore respectfully requested.

In view of the foregoing it is respectfully submitted that the present claims, as currently amended, distinguish over the prior art. A notice to that effect is earnestly solicited. If the Examiner believes there are any further matters, which need to be discussed in order to expedite the prosecution of the present application, the Examiner is invited to contact the undersigned.

Respectfully submitted,
TUCKER ELLIS & WEST LLP

A handwritten signature in black ink, appearing to read 'Jay P. Ryan', is written over a horizontal line.

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